ABSTRACT OF THE DISCLOSURE

A method and apparatus for a microprocessor with a cache that has the advantages given by a victim cache without physically having a victim cache is disclosed. In one embodiment, a victim flag may be associated with each way in a set. At eviction time, the way whose victim flag is true may be evicted. However, the victim flag may be reset to false if a superceding request arrives for the cache line in that way. Another cache line in another way may then have its victim flag made true.